COL215 LAB 4

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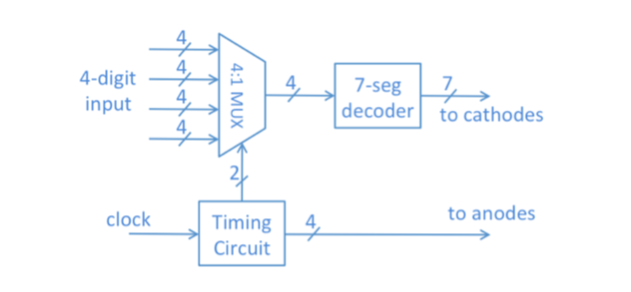
4 DIGIT SEVEN SEGMENT DISPLAY

Aim: To learn to use on-board clock and generate timing and refreshing signals .

Implementation :

We used 4 mutiplexers (always kept enabled) to take a 16 bit input and evaluate it to a 4 bit input fed into the previously designed Seven-Segment display of just 1 digit . We designed a timing circuit too comprising of 16 bit counter and a 2 bit counter driven by the custom clock . The last bit of 16 bit counter was used to run the 2 bit counter and the Q0 and Q1 outputs were fed to the S0 and S1 signals of all the multiplexers .

Each of the 4 inputs and the output of the multiplexer are 4 bits, representing a decimal or hexadecimal digit. The timing circuit has two roles – (a) it produces 2-bit select input for the multiplexer and (b) it produces signals for the anodes .The range of refresh period specified here is 1 ms to 16 ms. The clock frequency was kept in the range 250 Hz to 4KHz (4 times the refresh rate). This clock was generated from the on-board 100 MHz clock .



Circuit Diagram

Test cases

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| S.no | Sw0 | Sw1 | Sw2 | Sw3 | Sw4 | Sw5 | Sw6 | Sw7 | Sw8 | Sw9 | Sw10 | Sw11 | Sw12 | Sw13 | Sw14 | Sw15 | output |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 11 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 9 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |